Junior Verification Engineer

The ideal candidate will have following skills and background:

M. Sc. EE or equivalent degree in Electronics, Informatics, Computer Science, Automatic, Telecommunications or Electrical engineering.
Highly motivated and dynamic engineer able to adopt new technology quickly.
Familiar with C/C++ and computer architecture.

Additional skills that would be a plus are:

Familiar with scripting tools and languages (e.g. bash, csh, awk, Perl).
Familiar with software/hardware development tools (e.g. make and versioning tools (e.g. CVS/SVN).
Knowledge of C/C++ language and/or SystemC.
Familiar with complex flows for System-on-Chip projects.

Your key responsibilities would be:

Involvement in all stages of complex SoC verification including specification, test-bench design, verification plan, development, verification execution and verification sign off.
Proactive collaboration with team members in different locations
Review of the verification environment architecture and implementation specifications.

We offer:

For all junior engineers there will be 4-6 months technical training. It will be organized in HDL DH premises, executed by senior engineer with teaching experience from the Faculty of Electrical Engineering. The training will be organized based on Cadence (Incisive/X-Celium, Genus, Innovus, Tempus) and Mentor (QuestaSim) EDA tools.
During the training period, the junior engineers will not have other assignments and they will have fully paid salary.
Possibility of working from HDL DH Thessaloniki chip design center for a certain period of time
Unique chance to join a rapidly expanding company offering fantastic career and skills development opportunities, as well as an exceptional salary
Permanent employment, private health insurance and additional benefits
Opportunity to be part of many sports and team building activities with colleagues
Opportunity to travel abroad and work on our clients' cites
Working in young and enthusiastic team

Successful training completion and testing will be condition for candidates to join larger team working in all stages of complex SoC design and verification.

For all candidates proficient knowledge of UNIX/Linux and fluent English is a prerequisite!

Please send your CV to jobs@hdl-dh.com