KATARINA RADINOVIĆ KAPRALOVIĆ

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WORK EXPERIENCE

MAR – MAY 2018 **Embedded Systems Engineering Intern**
Comtrade Solution Engineering (www.comtrade.com)
- Implemented signal processing algorithm on the Cortex M0+ in C

JUL 2017 **Analog IC Design Intern**
HDL Design House (www.hdl-dh.com)
- Schematics and layout design of an operational amplifier in TSMC 28nm technology in Cadence Virtuoso

NOV 2016 – AUG 2018 **Assistant Laboratory Engineer**
Idvorsky Laboratories (www.idvorski.com)
- Electromagnetic compatibility testing: conducted and radiative emission and susceptibility

NOV 2015 – SEP 2018 **Undergraduate Teaching Assistant**
University of Belgrade, School of Electrical Engineering
- Engaged in courses 'Laboratory Experiments in Fundamentals of Electrical Engineering', 'Elements of Electronics' and 'Fundamentals of Digital Electronics' - examined students entering the lab, preparing experiments, validating instruments and general laboratory maintenance

EDUCATION

2014 – 2018 **University of Belgrade, School of Electrical Engineering, Department for Electronics**
Bachelor of Science
- Bachelor thesis: Implementation of 1D wavelet transform on FPGA
- GPA: 9.8
- Most relevant courses: Digital Electronics, Introduction to Integrated Circuit Design, Introduction to VLSI Systems Design, Digital Signal Processing, Digital Image Processing

PROFESSIONAL SKILLS

- VHLD, Verilog HLD
- C, C++, Python
- Altium
- PSpice
- Cadence Virtuoso
- Matlab

SOFT SKILLS

- Teamwork
- Organisational skills
- Responsibility
- Interpersonal skills
- Positive attitude

LANGUAGES

- English – level C1 (British Council certificate)
- German – A2
- Italian – A1

PROJECTS

AUG – SEP 2018 **Implementation of 1D wavelet transform on FPGA**
Bachelor thesis
- Implemented wavelet transformation using FIR filter banks in polyphase architecture
- Used VHDL

MAY 2018 **Pager**
Part of University course 'Integrated Computer Systems'
- Using TI MSP430F5438A microcontroller, Hitatchi LCD and GSM2 click module
- Software in C and assembly

JAN – FEB 2018 **Renesas MCU Car Rally**
Team competition – team of 6
- Contributed to the design of software in C++ driving an MCU car model detecting white line on the track
- Implemented part of the software enabling MCU car to overcome a specific segment of the track – lane change

NOV – DEC 2017 **Double click counter**
Part of University course 'Introduction to VLSI Systems Design' – team of 2
- Programmed FPGA chip in VHDL to count the number of double clicks on a taster on the chip and to send the data using SPI protocol to 8x8B click module

MAR – JUN 2017 **Configurable integrated IIR filter**
Part of University course 'Introduction to Integrated Circuits Design' – team of 2
- Designed filter in Cadence Virtuoso, full custom, in TSMC 180nm technology

JAN 2016 **Data flow machine**
Part of University course 'Object oriented programming'
- Implemented data flow machine for simple arithmetical calculations in C++

AWARDS

OCT 2017 3rd place at the twelfth annual international microelectronics olympiad of Armenia

DEC 2017 The best student in generation on the fourth, third and the second year of studies at Department for Electronics
DEC2016
DEC2015